

FIG. 1A  
(Prior Art)

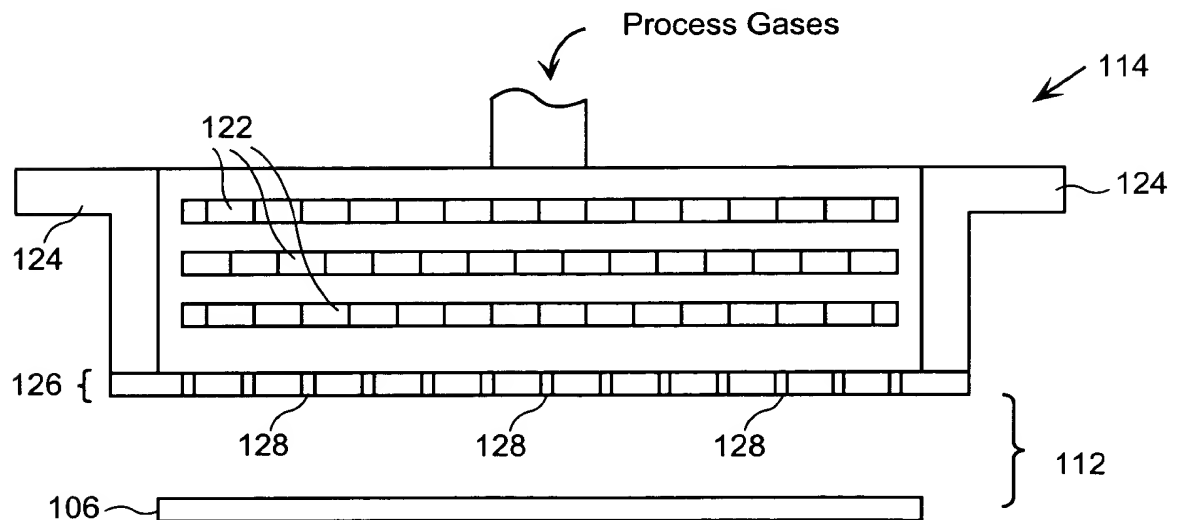
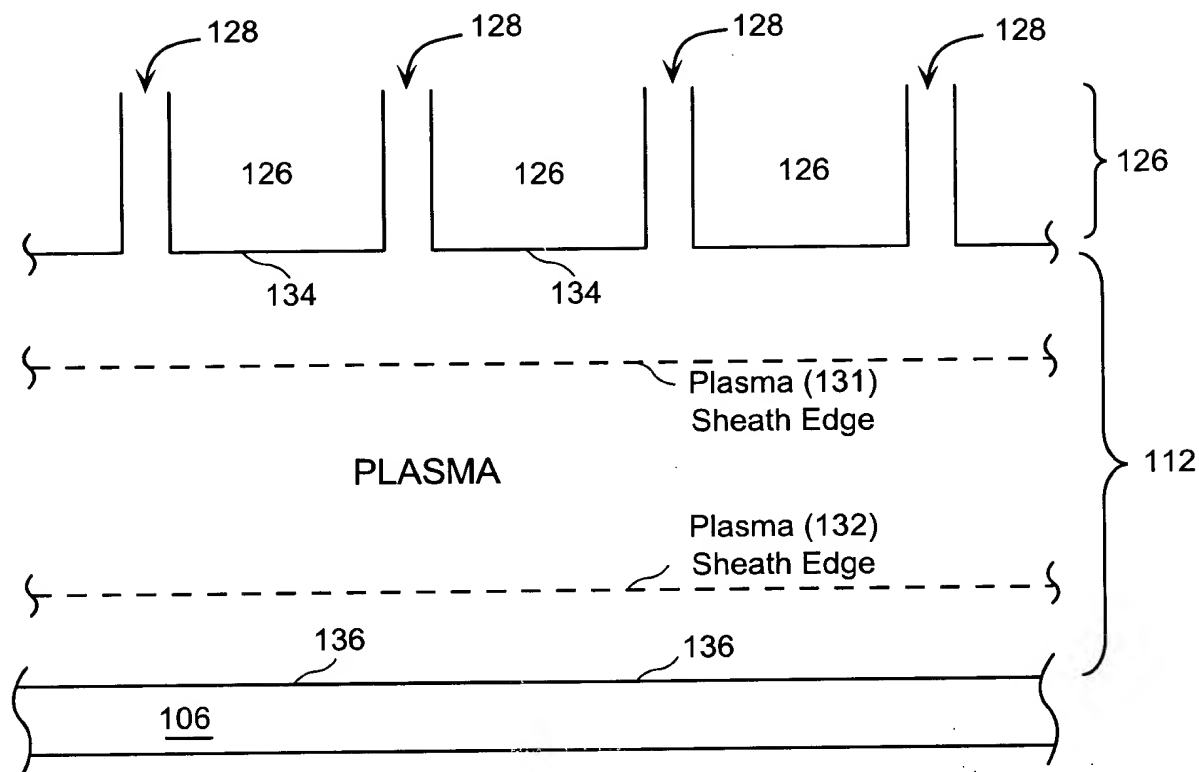


FIG. 1B  
(Prior Art)



**FIG. 1C**  
**(Prior Art)**

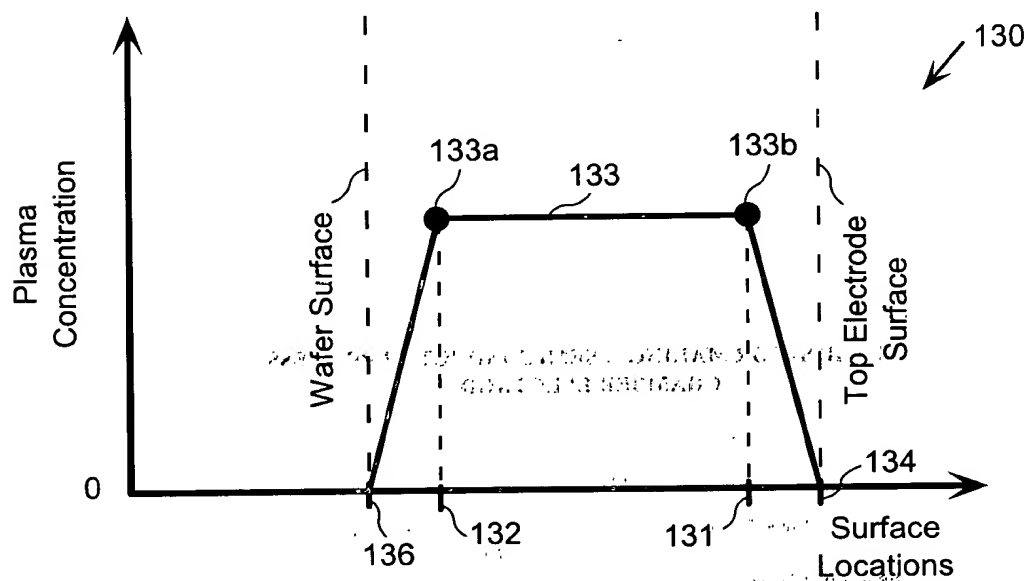


FIG. 1D  
(Prior Art)

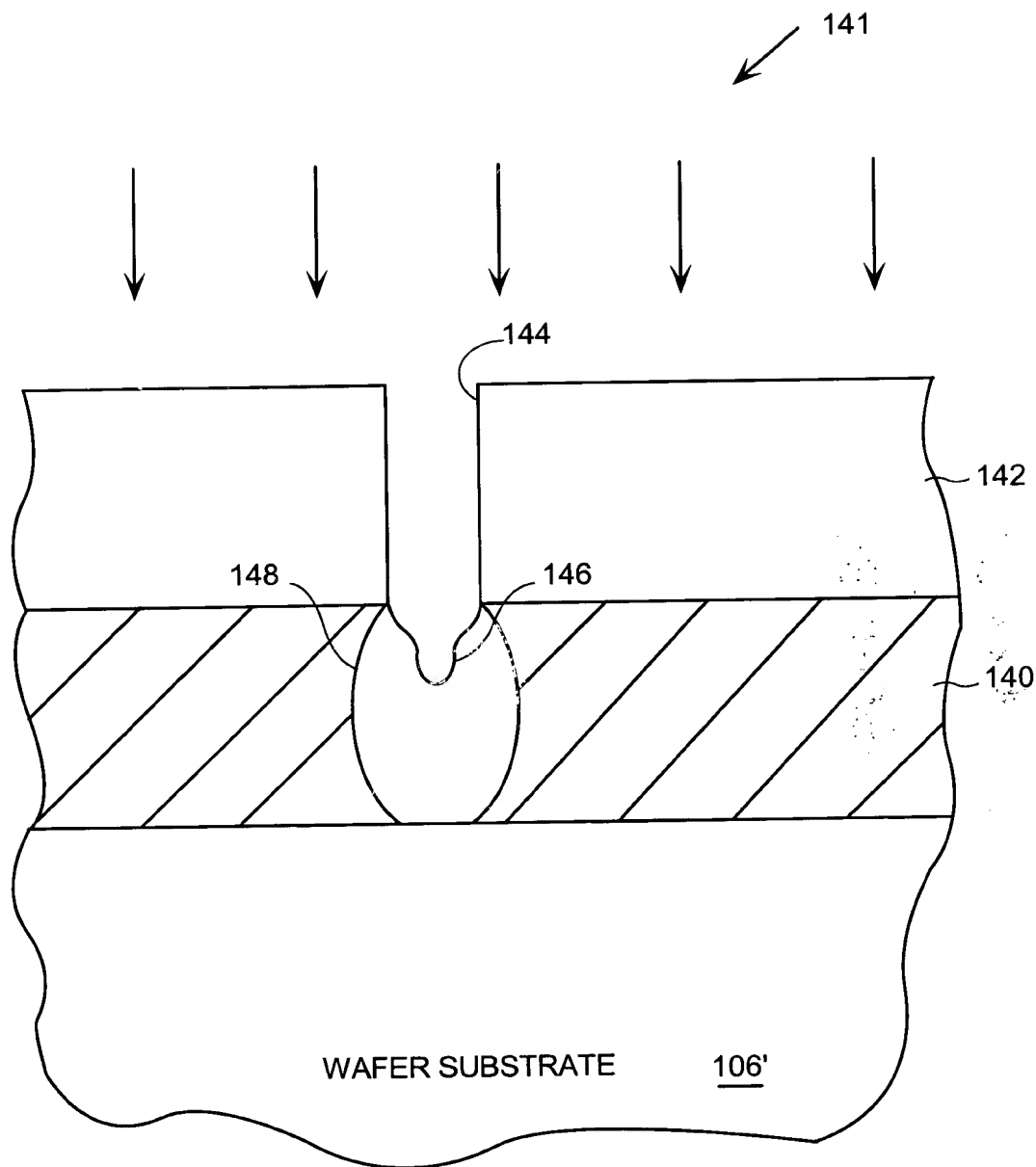


FIG. 1E  
(Prior Art)

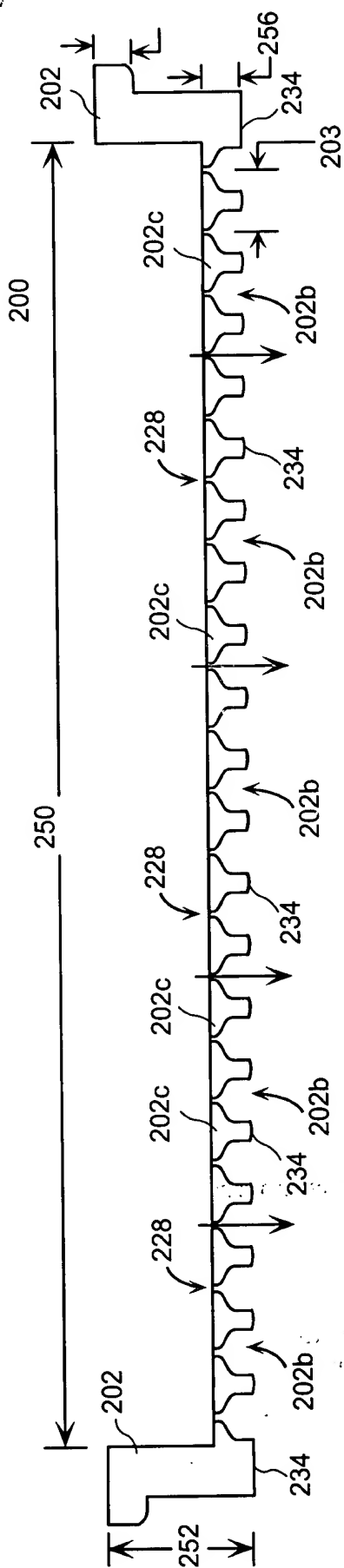


FIG. 2A

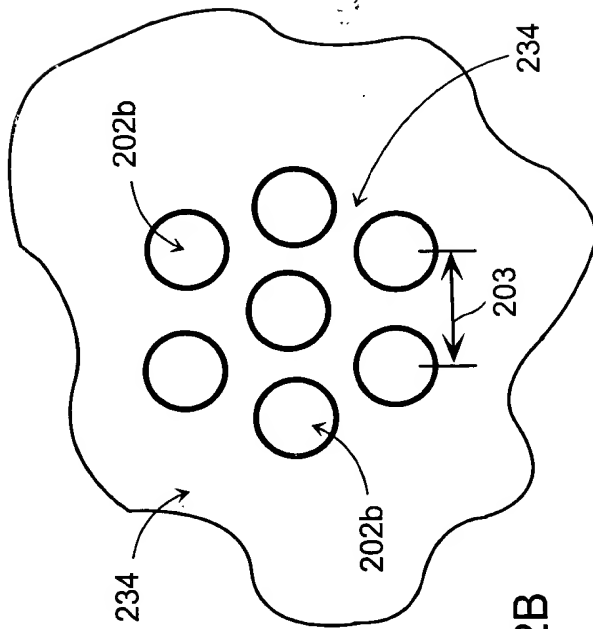


FIG. 2B

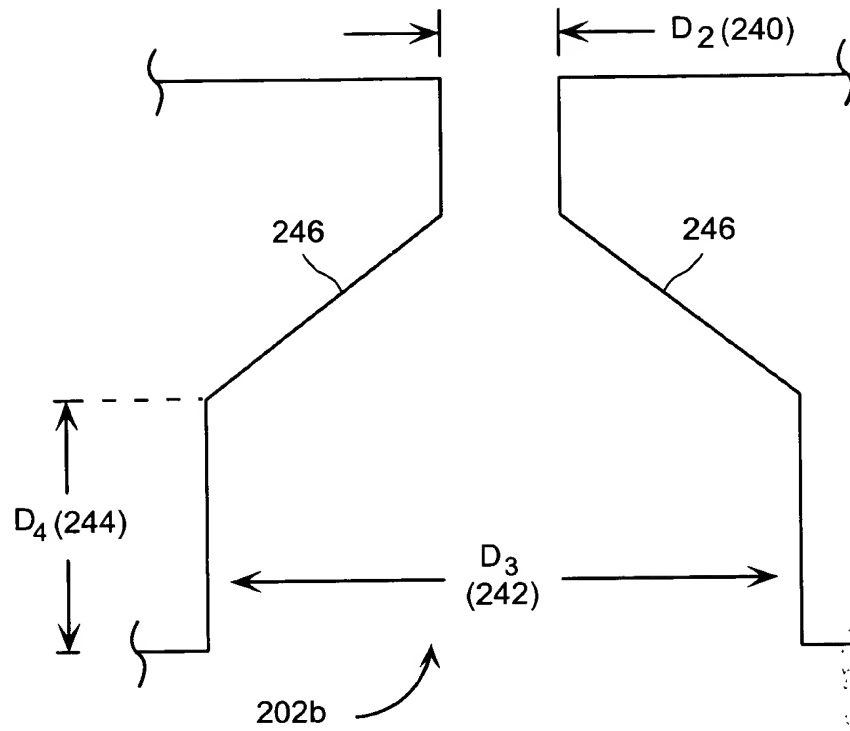


FIG. 2C

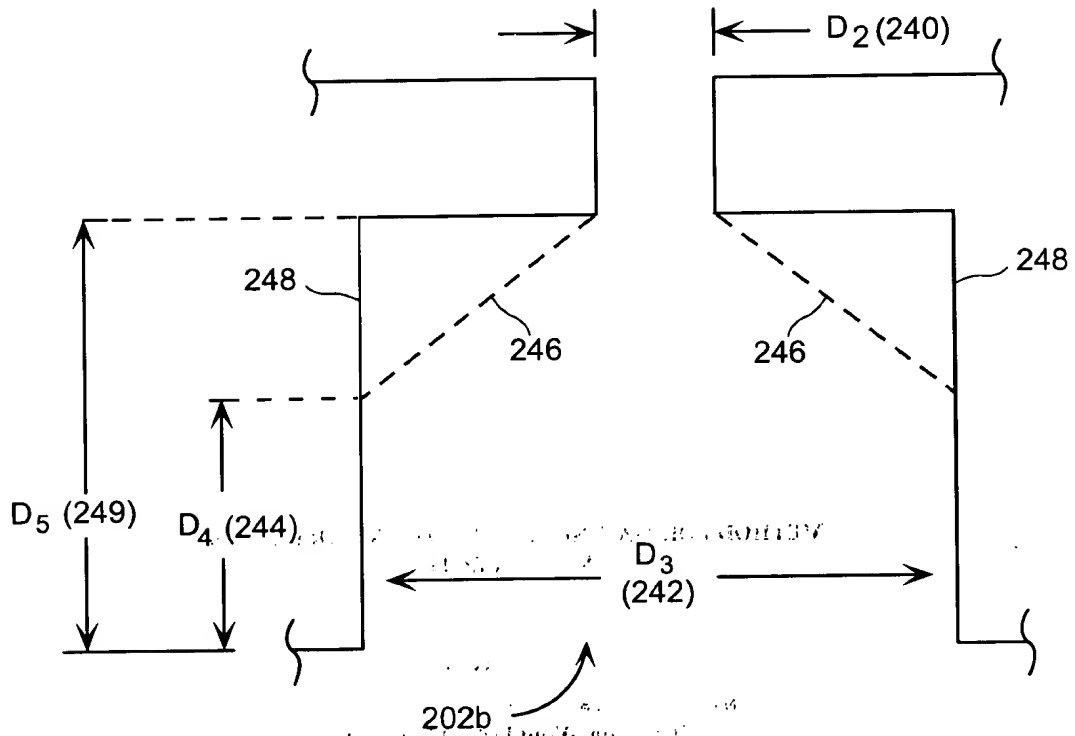


FIG. 2D

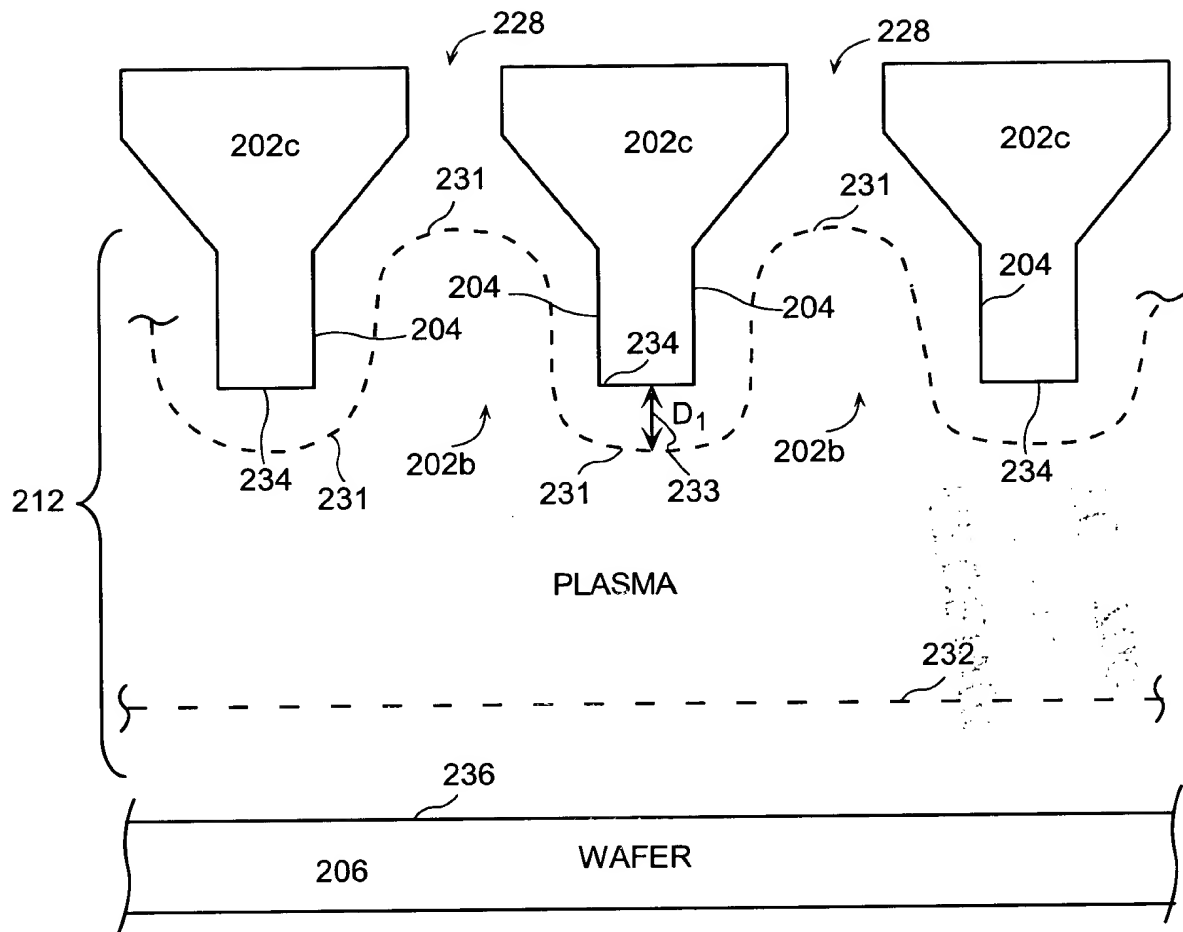


FIG. 2E

FIG. 2E is a schematic diagram of a plasma processing system.

The system includes a plasma source 202c, a central electrode assembly 204, and a wafer 206. The electrode assembly 204 includes a top flange 231 and a lower electrode 234. A dashed line 202b indicates a boundary or interface. A vertical arrow D1 points downwards from the electrode 234. The space between the chambers is labeled PLASMA. Below the chambers, a horizontal dashed line is labeled 232. At the bottom, a thick horizontal bar represents the WAFFER, labeled 206. A bracket on the right labeled 236 indicates the wafer area.

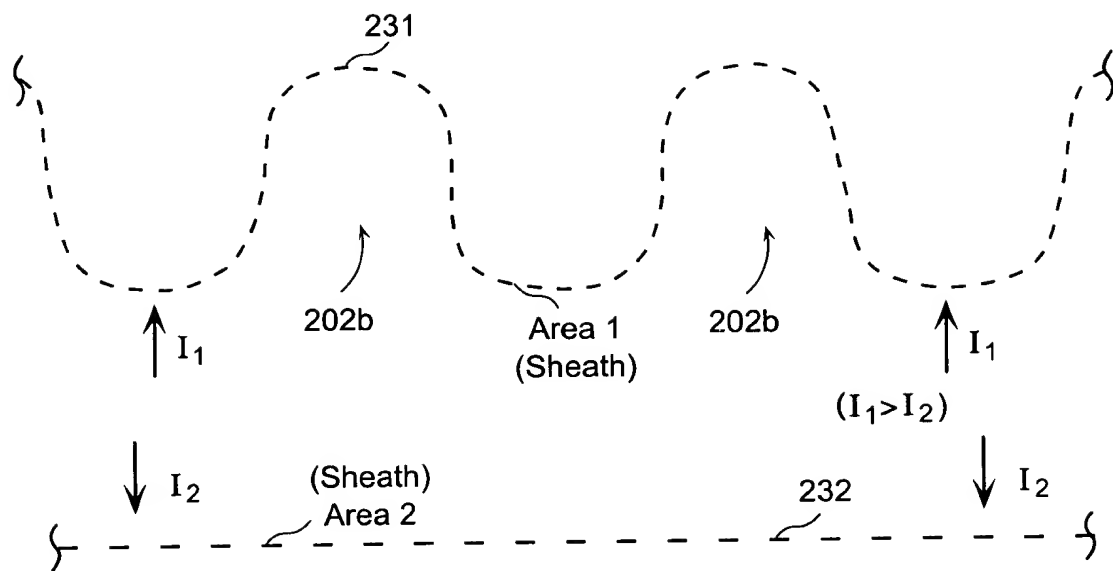


FIG. 3

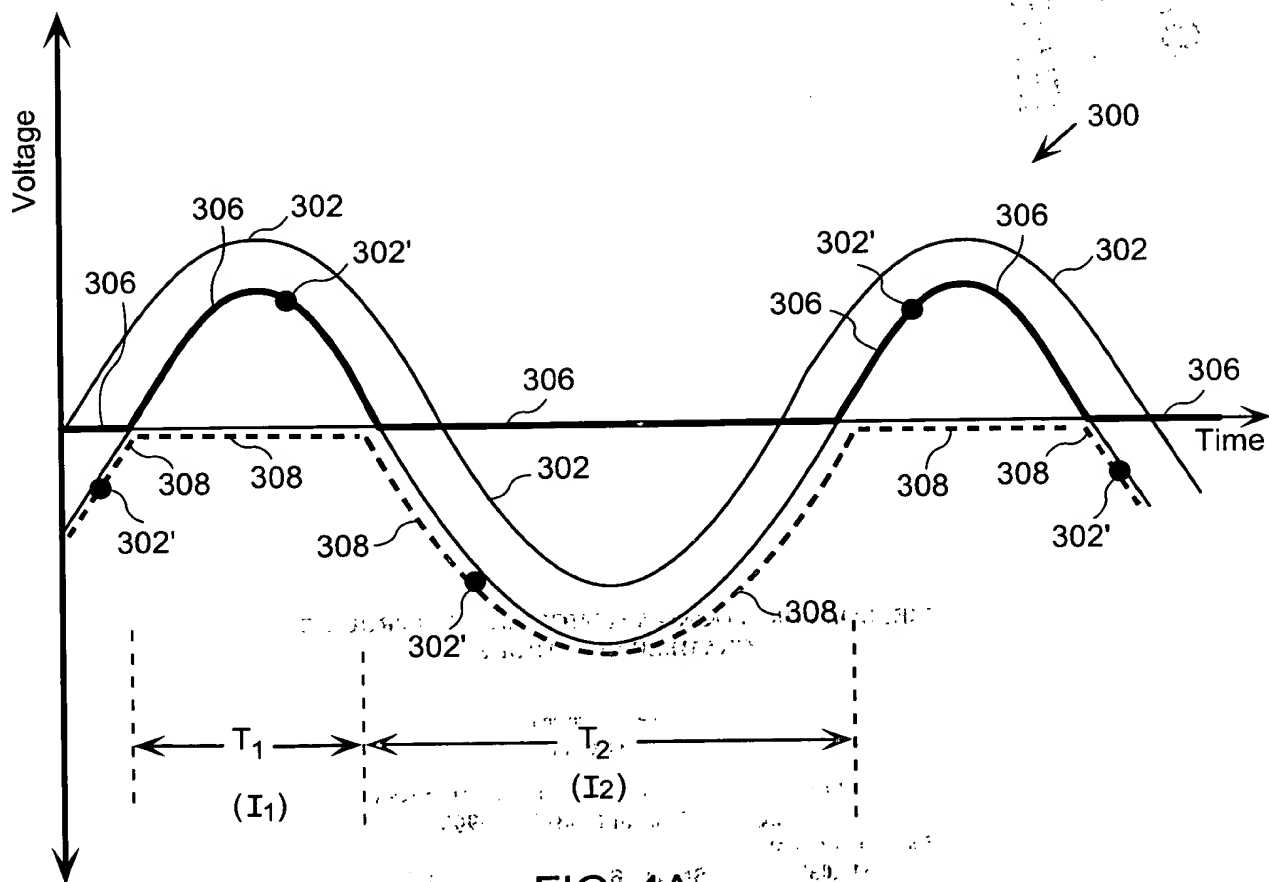


FIG. 4A

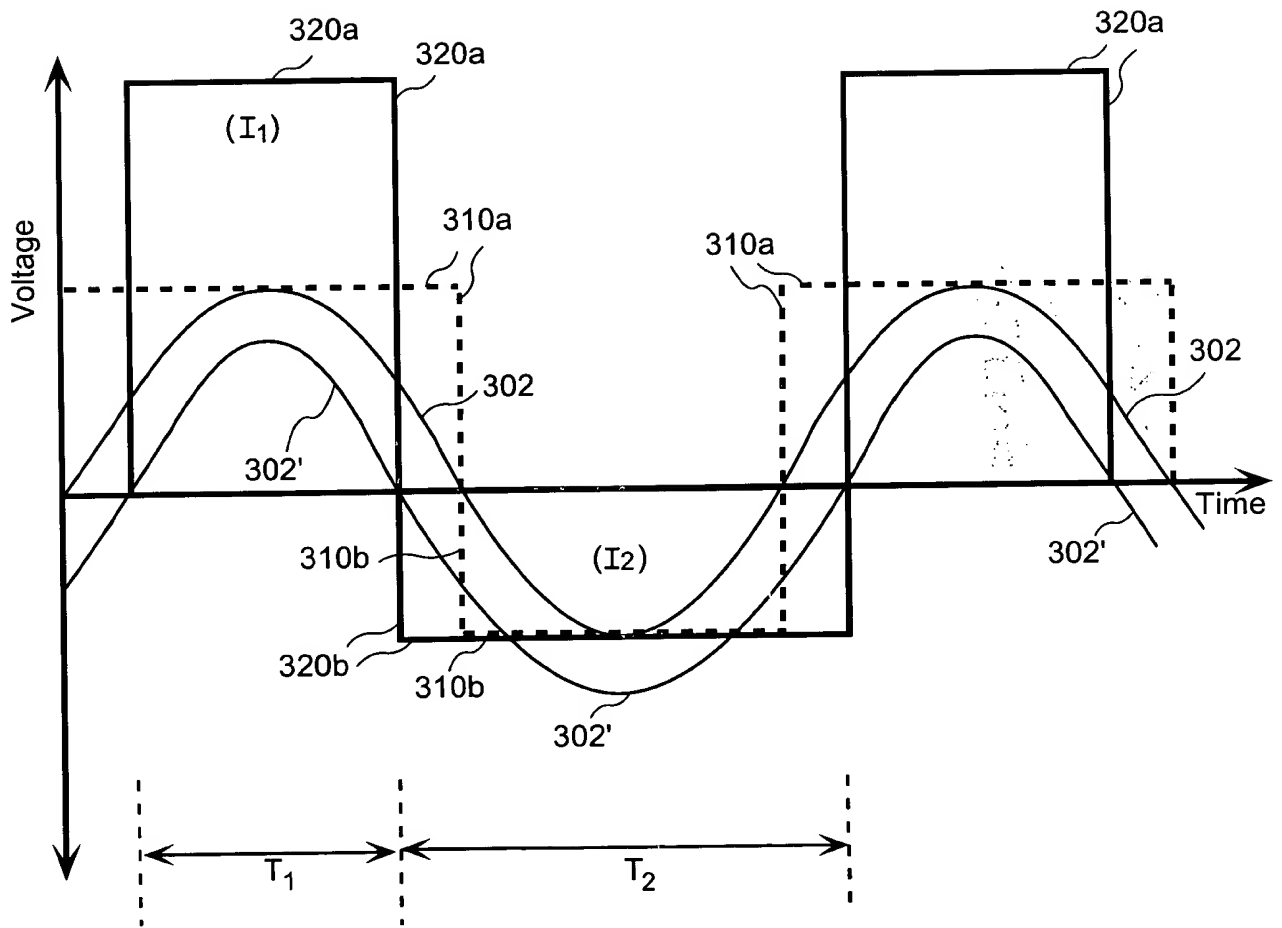


FIG. 4B





## Bias vs. Area Ratio

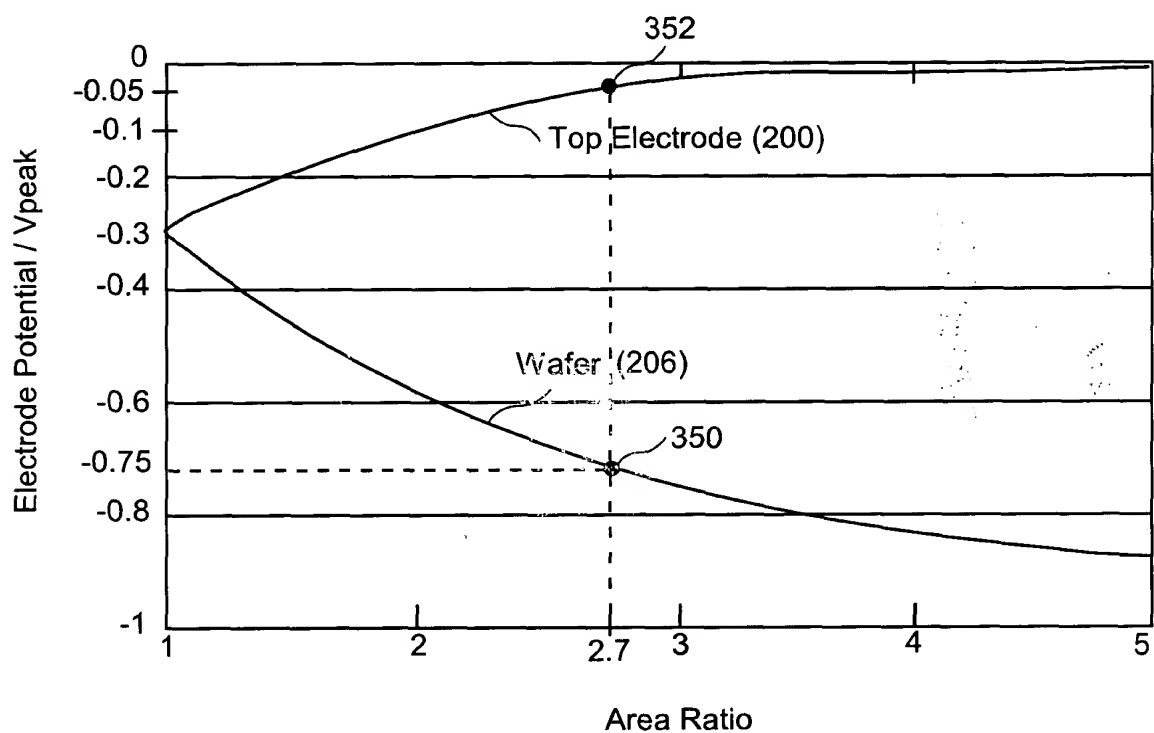


FIG. 5